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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,803	01/13/2004	Chao-Cheng Lee	REAP0003USA	1802

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EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,803	LEE ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19 and 20* is/are allowed.

6)☒ Claim(s) *1-18 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application No. 10/707803 filed on 08/11/05. Claims 1 – 20 are pending on this application.

Response to Arguments

2. Applicant's arguments, with respect to claims 1 and 7 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made from the following.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 14 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Callicotte et al. U.S. Patent No. 6,573,785.

Regarding claim 14, Fig. 5 of Callicotte et al. discloses a circuit comprising: a differential amplifier (510 comprising a positive input end (502), a negative input end (504), a positive output end (532), and a negative output end (542); a first input

impedance (514) coupled between the negative input end and a first input signal (Vinp); a second input impedance (524) coupled between the positive input end and a second input signal (522); a first output impedance (533) coupled between the negative input end (502) and the positive output end (532); a second output impedance (534) coupled between the negative input end (502) and the negative output end (542); a third output impedance (544) coupled between the positive input end (504) and the positive output end (532) the third output impedance being substantially equivalent to the second output impedance (544 and 534 having the same capacitances value "CR" therefore 544, and 534 having the same impedance value); and a fourth output impedance (543) coupled between the positive input end (504) and the negative output end (542), the fourth output impedance being substantially equivalent to the first output impedance (543 and 533 having the same capacitance value "CF"; therefore, 543 and 533 having the same impedance value), wherein resistances of the first and second output impedances (533, 534) are controlled by a first and a second control signals (Φ1, Φ2) respectively.

Regarding claim 18, wherein the first output impedance (533) is a switched capacitor circuit, the switched capacitor circuit comprises: a capacitor (Cf) coupled between a first node (532) and a ground end (564); a first switch (535) with one end coupled to the first node (532) and another end used as an end of the switched capacitor circuit; and a second switch (546) with one end coupled to the first node (532) and another end used as another end of the switched capacitor circuit, wherein the first switch and the second switch are turned on alternately by the first control signal (Φ).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 3, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulati et al. Pub.No.: US 2003/0146786 Anderson U.S. Patent No. 5,493,246.

Regarding claim 1, Fig. 6 of Gulati et al. discloses a circuit comprising: an operational amplifier (162) comprising a positive input end (positive input terminal of 162), a negative input end (Negative Input terminal of 162), and an output end (output terminal of 162); a first input impedance (C1+) coupled between the negative input end and a first input signal (Vin+); a second input impedance (C1-) coupled between the negative input end and a second input signal Vin-); and a first output impedance (Cf+) coupled between the negative input end and the output end, wherein resistances of the first and second input impedances are controlled by a first and a second control signals respectively (see controlling switches CL1, CL2 for controlling the resistance value of the first C1+ and second C- input impedance). However, Gulati et al. does not explicitly disclose the resistances of the first and second impedances are substantially different from each other from the controlling signals.

Fig. 1 of Anderson disclosing a differential amplifier (14) having first input impedance (12), second input impedance (18), first output impedance (22), and second output impedance, wherein the input and output impedances are form by programmable switching capacitors (Fig. 2), which user may changing the switching setting to adjust impedance values around the amplifier to achieve the desired impedance (Col. 2 lines 10 – 20).

Gulati et al. and Anderson are common subject matter for input and output of switching impedances for the differential amplifier circuit. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the concept programmable impedance taught by Anderson into programmable impedance of Gulati et al. for the impedance blocks to achieve the desired function (Anderson; Col. 2 lines 38 – 40).

Regarding claim 2, Gulati et al. as applied to claim 1 above, further discloses wherein resistances of the first and second input impedances are close to each other (both input impedance had the same value C1 therefore the resistance value of both inputs is the same).

Regarding claims 3 and 5, Gulati incorporated the controlling impedance to achieve the desired impedance of the impedance circuit taught by Anderson as applied to claim 2 above, therefore the high input impedance or large time constant is within desired function concept of the impedance taught by Anderson.

Regarding claim 6, Gulati et al. as applied to claim 1 above, further discloses wherein the first input impedance (C1+) is a switched capacitor circuit (CL1, CL2), the

switched capacitor circuit comprises: a capacitor (C1+) coupled between a first node and a ground end (C1+ coupled between the ground end via S4 and left node of C1+); a first switch (S1) with one end coupled to the first node (left node of C1+) and another end (V1+) used as an end of the switched capacitor circuit; and a second switched (S2) with one end coupled to the first node (left node of C1+) and another end (Ground) used as another end of the switched capacitor circuit, wherein the first switch and the second switch (S1, S2) are turned on alternately by the first control signal (CL1, CL2).

7. Claims 7 – 10, 12, 13 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Yin et al. U.S Patent No. 6,437,720, in view of Anderson U.S. Patent No. 5,493,246.

Regarding claim 7, Fig. 3 of Yin et al. discloses a circuit comprising: a differential amplifier (40) comprising a positive input end (+), a negative input end (-), a positive output end (OUTn), and a negative output end (OUTp); a first input impedance (60 between 62/y1 and Vrefp) coupled between the negative input end (-) and a first input signal (Vrefp); a second input impedance (61 between 63/y1) coupled between the positive input end (+) and the first input signal (Vrefp); a third input impedance (60 between 62/y2 and Vrefn) coupled between the negative input end (-) and a second input signal (Vrefn); a fourth input impedance (61 between 63/y2) coupled between the positive input end (+) and the second input signal (Vrefn), the fourth input impedance being substantially equivalent to the first in- put impedance (Col. 5 lines 46 – 50); wherein resistances of the first and second input impedances are controlled by a first

and a second control signals respectively (53, 54, 62, 63). However, Yin et al. does not explicitly discloses the third input impedance being substantially equivalent to the second input impedance; and the fourth input impedance being substantially equivalent to the first in- put impedance.

Fig. 1 of Anderson disclosing a differential amplifier (14) having first input impedance (12), second input impedance (18), first output impedance (22), and second output impedance, wherein the input and output impedances are form by programmable switching capacitors (Fig. 2), which user may changing the switching setting to adjust impedance values around the amplifier to achieve the desired impedance (Col. 2 lines 10 – 20).

Gulati et al. and Anderson are common subject matter for input and output of switching impedances for the differential amplifier circuit. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the concept programmable impedance taught by Anderson into programmable impedance of Gulati et al. for the impedance blocks to achieve the desired function (Anderson; Col. 2 lines 38 – 40).

Regarding claims 8, 9 and 21, the claims incorporated the same subject matter as of claim 7 for impedances characteristics, and rejected along the same rationale.

Regarding claim 10, Fig. 3 of Yin et al. combined with Anderson as applied to claim 7 above further comprising: a first output impedance (77) coupled between the negative input end (-) and the positive output end (+); and a second output impedance (80) coupled between the positive input end (+) and the negative output end (-).

Regarding claim 12, Yin et al. incorporated the controlling impedance to achieve the desired impedance of the impedance circuit taught by Anderson as applied to claim 7 above, therefore large time constant is a one desired function of the switching capacitor impedance taught by Anderson.

Regarding claim 13, Yin et al/ Anderson as applied to claim 7 above further discloses the first input impedance of his is a switched capacitor circuit (Fig. 7), and the switched capacitor circuit comprises: a capacitor (60) coupled between a first node (51) and a ground end (72) a first switch (53) with one end coupled to the first node and another end used as an end of the switched capacitor circuit; and a second switch (57) with one end coupled to the first node and another end used as another end of the switched capacitor circuit, wherein the first switch and the second switch are turned on alternately by the first control signal (Φ).

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gulati et al./Anderson as applied to claim 2 above, in view of Sobel U.S. Patent 6,833,759.

Gulati et al. as applied to claim 2 above, does not disclose wherein the first output impedance is a resistive-impedance, the circuit has a high voltage attenuation characteristic.

Fig. 4 of Sobel discloses a differential amplifier circuit having the first output impedance is a resistive-impedance (401) with high voltage attenuation characteristic (406a1- 406an).

Gulati et al. and Sobel are common subject matter for controlling impedance of differential amplifier circuit. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the resistive output impedance taught by Sobel incorporated into the output impedance of Gulati et al. for the purpose of providing passive attenuation therefore the total complexity of the feedback of the amplifier can be reduced (Sobel, Col. 4 lines 1 – 8).

8. Claim 11, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yin/Anderson as applied to claim 10 above, in view of Sobel U.S. Patent 6,833,759

Regarding claim 11, Yin/Anderson as applied to claim 10 above, does not disclose wherein the first output impedance is a resistive-impedance, the circuit has a high voltage attenuation characteristic.

Fig. 4 of Sobel discloses a differential amplifier circuit having the first output impedance is a resistive-impedance (401) with high voltage attenuation characteristic (406a1- 406an).

Yin et al./Anderson and Sobel are common subject matter for controlling impedance of differential amplifier circuit. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the resistive output impedance taught by Sobel incorporated into the output impedance of Gulati et al./Anderson for the purpose of providing passive attenuation therefore the total complexity of the feedback of the amplifier can be reduced (Sobel, Col. 4 lines 1 – 8).

9. Claims 15 - 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callicotte et al. as applied to claim 14 above, in view Anderson U.S. Patent No. 5,493,246.

Regarding to claim 15, Callicotte et al. as applied to claim 14 above, does not explicitly discloses wherein resistances of the first (533) and the second (534) output impedance are close to each other.

Fig. 1 of Anderson disclosing a differential amplifier (14) having programmable output impedance (22, 24), wherein the output impedances are form by programmable switching capacitors (Fig. 2), which user may changing the switching setting to adjust impedance values around the amplifier to achieve the desired impedance (Col. 2 lines 10 – 20).

Callicotte et al. and Anderson are common subject matter for controlling input and output impedance of differential amplifier. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the concept programmable impedance taught by Anderson into programmable impedance of Callicotte et al. for the impedance blocks to achieve the desired function (Anderson; Col. 2 lines 38 – 40).

Regarding to claims 16 and 17, wherein at least one the first and the second input impedance is a resistive-impedance, the circuit has a high voltage gain characteristic or a capacitive-impedance, the circuit has a large time constant characteristic (Since the concept programmable switching capacitor impedance of Anderson to change the setting switches by user of input and output impedance block to

achieve the desired function of impedance blocks, therefore the large time constant or high resistive impedance of capacitors is within the concept of achieve the desired function of impedance taught by Anderson) .

Allowable Subject Matter

10. Claims 19 and 20 are allowed.

11. The following is an examiner's statement of reasons for allowance:

With respect to claims 19, in addition to other elements in each respective claim, the prior are doest not teach or suggest a differential amplifier having third input impedance coupled between the negative input end and a second input signal, the third input impedance being substantially equivalent to the second input impedance; a fourth input impedance coupled between the positive input end and the second input signal, a third output impedance coupled between the positive input end and the positive output end; and a fourth output impedance coupled between the positive input end and the negative output end, the fourth output impedance being substantially equivalent to the first output impedance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Prior Art

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Contact Information

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Robert Pascal can be reached at (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

10/2/05

Linh Van Nguyen 

Art Unit 2819